In-Situ Calibration: Migrating Control System IP Module Calibration from the Bench to the Storage Ring

J. M. Weber, M. Chin

Lawrence Berkeley National Laboratory, 1 Cyclotron Road, Berkeley, CA 94720

Abstract. The Control System for the Advanced Light Source (ALS) at Lawrence Berkeley National Lab (LBNL) uses in-house designed IndustryPack® (IP) modules contained in compact PCI (cPCI) crates with 16-bit analog I/O to control instrumentation. To make the IP modules interchangeable, each module is calibrated for gain and offset compensation. We initially developed a method of verifying and calibrating the IP modules in a lab bench test environment using a PC with LabVIEW. The subsequent discovery that the ADCs have significant drift characteristics over periods of days of installed operation prompted development of an "in-situ" calibration process--one in which the IP modules can be calibrated without removing them from the cPCI crates in the storage ring. This paper discusses the original LabVIEW PC calibration and the migration to the proposed in-situ EPICS control system calibration.

INTRODUCTION

The ALS Instrumentation Group designed custom IP Modules for the ALS Control System. Housed in cPCI crates, these modules control instruments such as magnet power supplies and beam position monitors (BPMs). Each IP Module consists of two 16-bit analog control channels (DACs) and four 16-bit analog monitor channels (ADCs). To make modules interchangeable and increase channel accuracy, each channel is calibrated for gain and offset compensation. We developed LabVIEW calibration software (IPCal) to calculate calibration constants for each channel and compile this data in a file. The file contains slope, offset, and mean-square-error (MSE) constants for each of the six channels on the IP module. Each IP module stores its calibration file in an onboard EEPROM. The ALS control system database uses the calibration constants to adjust data read from and written to each channel.

Originally, the test bench setup was sufficient to perform an initial calibration on each module before installing the modules into cPCI crates in the storage ring. We then discovered that many of the ADC channel offsets drifted several mV over weeks of installed operation. Further investigation revealed that the ADC channels exhibit an exponential drift from their initial offset as illustrated in Figure 1.

The ADC (ADS7825U) data sheet specifies a maximum zero offset error of $\pm 10 \text{mV}$ with a typical drift of $\pm 2 \text{ppm/}^{\circ}\text{C}$. ALS instrumentation and control requires a maximum drift of 10 mV/year. These specifications coupled with the measured drift prompted a recalibration of each installed module. To perform the recalibration, each module would have to be removed during a storage ring shutdown, recalibrated in the test bench environment, and reinstalled during the same or a subsequent shutdown. Moreover, future recalibration, verification, and troubleshooting necessitate access to the installed and operating IP modules.

IP ADC Offset Drift

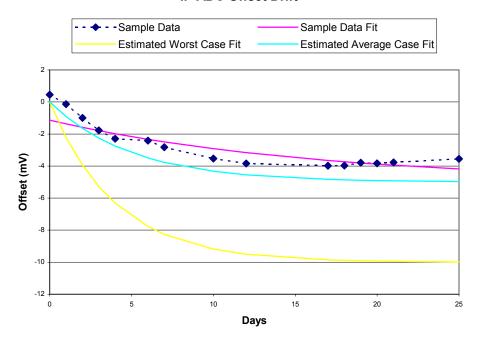


FIGURE 1. Plots show measured and estimated ADC offset drift. Estimated fits are based on testing a small sample of IP modules under varying conditions. Actual average and worst case offset drift of installed operating modules may differ. Assume initial offset of zero.

To improve the recalibration process, we are developing an in-situ calibration, wherein each module can be calibrated quickly and efficiently without being removed from the storage ring. Instead of powering down the cPCI crate, removing the IP modules, and disabling the corresponding instruments all at once, IP modules can be individually disabled to perform the in-situ calibration. This makes

the in-situ process flexible, fast, and minimally disruptive to storage ring instrumentation.

CALIBRATION METHOD

To calibrate an IP module, each DAC output is connected to two ADC inputs and to an analog input channel on an Agilent (HP) 34970a Data Acquisition Switch Unit. The calibration software (IPCal) configures the 34970 for 20 bit resolution on each analog scan. The PC reads the 34970 digital output via RS-232 after each scan.

The full scale range of each DAC and ADC is 16 bits representing -10 to \pm 10 Volts. IPCal writes to the DAC values from 0x1000 to 0xF000 (-8.75 to \pm 8.75 Volts) to avoid nonlinear behavior at the limits of the range. The DAC values are written in steps of 160 (0xA0) for a total of 358 steps.

To begin the calibration sequence, IPCal writes a value to the DAC. The output of each ADC connected to the DAC is sampled 10 times and averaged. Each average is stored in an array of ADC output values. Then the 34970 scans the analog (DAC output and ADC input) value which is also stored in an array. This cycle is repeated until the sample range has been exercised. After generating the arrays, IPCal calculates the calibration constants. This entire process is repeated for the other channel set (DAC and 2 ADCs). When calibration constants have been generated for both channel sets, IPCal writes these values to a calibration file stored locally on the PC.

After IPCal generates the calibration file, a simple verification is performed to ensure the IP module will operate within tolerance. When IPCal generates calibration constants for a channel set, it displays several plots used for manual verification. These plots show the following: the averaged and raw ADC output values; the difference between input and output for the DACs and ADCs at each sample point; the step size between each sample point. These plots allow the tester to visually check gain, offset, and linearity for each channel.

In a separate window, IPCal uses the calibration parameters to simulate the gain and offset compensation. The software allows the tester to write to the DAC in volts and monitor the bit patterns for the DAC input and the ADC output in both bits and calibrated volts. As a coarse gain and offset test, the tester can exercise the DAC input in one volt steps over the ± 10 Volt range and visually inspect the calibrated ADC. The software also allows access to the individual bits on the two 8-bit digital I/O ports. Each pin on port A is connected to port B across low value resistors (120Ω). The tester sets one port as input, the other as output and toggles each bit. This tests the data and control lines which could affect the results of the calibration if they are not working properly.

LABVIEW PC BENCH CALIBRATION

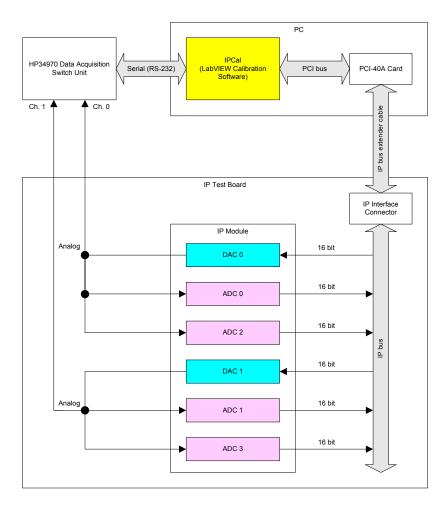


FIGURE 2. Block Diagram of the Test Bench Calibration.

Hardware

As shown in Figure 2, the bench calibration requires a PC with a PCI interface to the IP module and an RS-232 serial interface to the 34970. The PC contains an SBS Greenspring PCI-40A card with 4 slots for IP modules. For improved accessibility to the IP module and increased speed during the calibration process, we developed an in-house general purpose IP test board with hot swap capability and optional calibration configuration. This board allows us to probe both sides of the IP module during operation and swap IP modules without power cycling the PC. This board connects to the PCI card through an IP extender cable. The HP34970 accesses the IP module analog channels through BNC connectors on the IP test board.

Software

The IP module calibration is controlled at the highest level by LabVIEW software (IPCal). LabVIEW provides both PCI bus access and RS-232 serial control. LabVIEW interfaces to the PCI bus through BSquare (formerly Bluewater Systems) WinRT, a hardware driver that controls the PCI-40A card. This driver enables LabVIEW to access the digital signals on the IP module. LabVIEW controls the HP34970 with VISA functions via the serial port. VISA functions allow the user to control devices with uniform function calls via GPIB, RS-232, or Ethernet.

IN-SITU CALIBRATION

Hardware

Figure 3 shows the proposed in-situ calibration setup. The components of the in-situ calibration include a PC to run IPCal, an HP34970 Switching Unit, a breakout box for access to analog signals on the IP module, and a cPCI crate with a carrier board containing the IP module to be calibrated. The cPCI crate is located inside the storage ring and the PC and the 34970 are located on a mobile cart close to the cPCI crate. As in the bench calibration, the PC connects to the 34970 through a serial port. The PC communicates with the cPCI crate via Ethernet.

The ALS uses an in-house custom cPCI rear I/O card to interface IP modules to instruments. A test/breakout box with calibration configuration capability is being developed to interface the cPCI rear I/O connectors to the 34970. This breakout box will output the IP module analog signals via BNC connectors, enabling the 34970 to access these channels as in the bench calibration.

To perform an in-situ calibration, the cables from the cPCI crate to the controlled instrument are disconnected and the breakout box is inserted in series. This causes a temporary loss of operation for the controlled instrument. As such, an in-situ calibration may only be performed while the ALS is not operating with beam in the storage ring.

Software

The in-situ LabVIEW calibration software has the same user interface (IPCal) as the bench calibration software. Since the 34970 is still controlled by the PC through a serial interface, the VISA functions that control the 34970 remain the same. However, the in-situ software uses an ActiveX component to communicate with the cPCI chassis over the network.

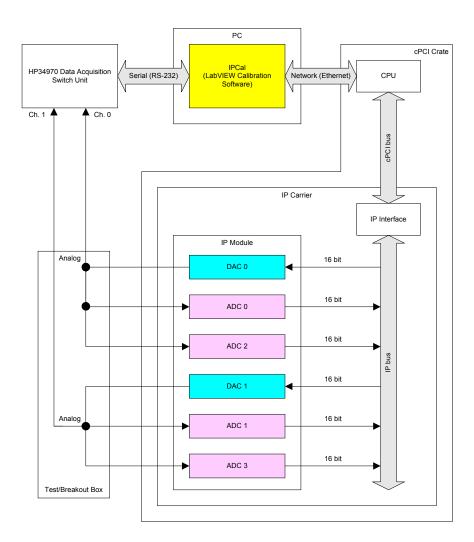


FIGURE 3. Block Diagram of the In-Situ Calibration.

The ALS control system EPICS records typically report values in engineering units (i.e. amps). Since the calibration software requires raw values (i.e. ± 32768 bits), the cPCI crate must be rebooted to replace the operating records with test records that report raw values.

LabVIEW uses ActiveX through Simple Channel Access (SCA), an EPICS tool used for network communication. SCA allows LabVIEW to invoke methods in the ActiveX component. The ALS Controls Group has developed custom methods to read and write values in EPICS records. With these methods, the calibration software can access the digital signals on the IP module.

SYSTEM RESULTS AND PERFORMANCE

The current test bench calibration software and hardware configuration will be used to benchmark system performance. This includes using a 400 MHz PC with 128MB RAM to run the calibration software. Since PC processor speed and memory impact LabVIEW application overhead, we base our comparison of the calibration systems on this PC. Table 1 gives a timing comparison for each calibration setup.

Table 1. Calibration Timing Comparison.

	Calibration Setup	
Operation	Bench (PC)	In-Situ (cPCI)
ADC Read	0.38 ms	2.32 ms
DAC Write	0.26 ms	4.46 ms
HP34970 Read Setup Delay	100 ms	100 ms
HP34970 Read	100 ms	100 ms
Single Calibration Cycle (1 Write, 10 Reads, 34970)	210 ms	390 ms
Single Channel Set Calibration	1.30 min	2.40 min
Generate Calibration File	2.70 min	4.90 min

In the test bench environment, there are two significant timing factors: the 100ms HP34970 read setup delay, and the 100ms HP34970 read. These factors account for the majority of the calibration cycle time. In the in-situ calibration, the significant timing factors are the HP34970 read setup delay, the HP34970 read, the ADC read, and the DAC write. The HP34970 read time remains the same because the default resolution is used in both setups. The most significant timing differences between the two setups is in the ADC Read and DAC Write. This difference stems from communicating over the network instead of over the PCI bus in the PC. The ALS uses high speed 100Mbps Ethernet, which is still slower than the PCI bus in the PC.

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